Our Docket No.: 042390.P3495C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael Barrow

Application No.: 08/959,546

Filed: October 24, 1997

For: **PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A POPULATED CENTER**

Examiner: J. Foster

Art Group: 2103

DECLARATION OF MICHAEL BARROW UNDER 37 C.F.R. §1.131

Assistant Commissioner for Patents
Washington, DC 20231-9998

Sir:

I, Michael Barrow, hereby declare that:

1. I am the named inventor for the above-entitled patent application.

2. The above-entitled patent application discloses and claims a ball grid array package which has an outer array of contact pads and a center array of contact pads on a bottom surface of the package. The arrays of contact pads are separated by a distance that is greater than the distance which separates the pads within the arrays. Solder balls are attached to the contact pads of the package.

3. Prior to April of 1995, I conceived the ball grid array package disclosed and claimed in the above-entitled patent application.

4. The conception of the above-entitled patent application was shown in a document entitled "Orion Chipset & Orion-DT Chipset Electrical Mechanical and Thermal Specification (EMTS), true copies of portions of the EMTS are attached as Exhibit A. The EMTS was prepared prior to April of 1995.

5. Page 2 of Exhibit A is a drawing which shows the claimed ball grid array package of the above-entitled patent application. The drawing shows a package which has a center array, an outer array and a space which separates the arrays. The space has a distance which is greater than a distance which separates the contact pads of an array. The drawing also discloses solder balls attached to the package.

6. A prototype of the package shown on page 2 of Exhibit A was built and reduced to practice prior to April of 1995.

7. The claimed invention was conceived in the United States prior to April of 1995, and a prototype which represented a reduction to practice of the invention existed in the United States prior to April of 1995.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 4/28/98

Michael Barrow

Orion Chipset
& Orion-DT Chipset
Electrical Mechanical and Thermal Specification (EMTS)

Version 2.0
(Review Copy)

Intel Corporation
042390.P3495C
08/959,546
Exhibit A

6.0 BGA Package Dimensions

6.0.1 OPB: 352 pin BGA

Note: Shaded pins in Table 6.1 are "reserved" in the Orion-DT Chipset only.